SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

This application is based upon and claims the benefit of priority from Japanese Patent Application No. 2015-179327; filed on September 11, 2015; the entire contents of which are incorporated herein by reference.

FIELD

Embodiments described herein relate generally to a semiconductor device.

BACKGROUND

In a vertical device which includes electrode on a front surface and a rear surface of a semiconductor device, a termination structure such as a RESURF or a guide ring is provided in the periphery of an element region in order to increase a breakdown voltage. By providing a termination region, electric field concentration at an end portion of the element region is reduced, and avalanche breakdown is prevented from occurring at the end of the element region.

It is preferable that a device in which avalanche breakdown does not occur at the end portion of the element region is designed, from a viewpoint in which avalanche resistance of a vertical device increases. If the avalanche breakdown occurs at the end of the element region, element breakdown easily occurs, compared to a case in which avalanche breakdown occurs inside the element region.

An example of related art includes JP-A-2014-204038.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic sectional view of a semiconductor device according to a first embodiment.

FIG. 2 is a schematic planar view of the semiconductor device according to the first embodiment.

FIG. 3 is a schematic sectional view of a semiconductor device according to a second embodiment.

FIG. 4 is a schematic sectional view of a semiconductor device according to a third embodiment.

FIG. 5 is a schematic sectional view of a semiconductor device according to a fourth embodiment.

FIG. 6 is a schematic planar view of a semiconductor device according to a fifth embodiment.

FIG. 7 is a schematic sectional view of a semiconductor device according to a sixth embodiment.

FIG. 8 is a schematic sectional view of a semiconductor device according to a seventh embodiment.

FIG. 9 is a schematic sectional view of a semiconductor device according to an eighth embodiment.

DETAILED DESCRIPTION

[0005]Exemplary embodiments provide a semiconductor device which can increase avalanche resistance.

[0006]In general, according to one embodiment, a semiconductor device includes a SiC layer which includes a first surface and a second surface; a first electrode which comes into contact with the first surface; a first SiC region of a first conductive type which is provided in the SiC layer; a second SiC region of the second conductive type which is provided in the SiC layer such that at least a part of the second SiC region surrounds a region which comes into contact with the first electrode and the first surface, and is provided between the first SiC region and the first surface; a third SiC region of a second conductive type which is provided in the SiC layer so as to surround the second SiC region, is provided between the first SiC region and the first surface, and contains lower impurity concentration of the second conductive type than that of the second SiC region; and a fourth SiC region of the second conductive type which is provided in the SiC layer between the second SiC region and the third Sic region, and contains higher impurity concentration of the second conductive type than that of the second SiC region.

[0008]Hereinafter, embodiments of the invention will be descried with reference to the drawings. In the following description, the same symbols or reference numerals will be attached to the same or similar members or the like, and description of the members or the like described once will be appropriately omitted.

[0009]In addition, in the following description, notation of n+, n and n-, and p++, p+, p and p- represents relative levels of impurity concentrations of each conductive type. That is, it represents that n+-type impurity concentration is relatively higher than n-type impurity concentration, and n--type impurity concentration is relatively lower than n-type impurity concentration. In addition, it represents that p++-type impurity concentration is relatively higher than p+-type impurity concentration, p+-type impurity concentration is relatively higher than p-type impurity concentration, and p--type impurity concentration is relatively lower than p-type impurity concentration. There is a case in which n+ and n- are simply described as an n-type, and p++, p+ and p- are simply described as a p-type.

First Embodiment

[0010]A semiconductor device according to the present embodiment includes a SiC layer which includes a first surface and a second surface; a first electrode which comes into contact with the first surface; a first SiC region of a first conductive type which is provided in the SiC layer; a second SiC region of the second conductive type which is provided in the SiC layer such that at least a part of the second SiC region surrounds a region which comes into contact with the first electrode and the first surface, and is provided between the first SiC region and the first surface; a third SiC region of a second conductive type which is provided in the SiC layer so as to surround the second SiC region, is provided between the first SiC region and the first surface, and contains lower impurity concentration of the second conductive type than that of the second SiC region; and a fourth SiC region of the second conductive type which is provided in the SiC layer between the second SiC region and the third Sic region, and contains higher impurity concentration of the second conductive type than that of the second SiC region.

[0011]FIG. 1 is a schematic sectional view of a semiconductor device according to a first embodiment. FIG. 2 is a schematic planar view of the semiconductor device according to the first embodiment. FIG. 2 illustrates a pattern of impurity region on a SiC layer. FIG. 1 illustrates a cross section taken along line I-I of FIG. 2. The semiconductor device according o the present embodiment is a Schottky barrier diode (SBD) 100.

[0012]The Schottky barrier diode 100 includes an element region and a termination region which surrounds the element region. The element region functions as a region through which a current mainly flows at the time of a forward bias of the Schottky barrier diode 100. The termination region includes a termination structure in which strength of an electric field which is applied to an end portion of the element region is reduced, a breakdown voltage of the end portion of the element region increases, and avalanche resistance of the Schottky barrier diode 100 increases, at the time of a forward bias of the Schottky barrier diode 100.

[0013]The Schottky barrier diode 100 includes a SiC layer 10, an anode electrode (first electrode) 12, a cathode electrode (second electrode) 14, and a field oxide film 16. In the SiC layer 10, an n+-type cathode region 18, an n--type drift region (first SiC region) 20, a p+-type edge region (second SiC region) 22, a first RESURF region of a p-type (third SiC region) 24, a second RESURF region of a p--type (fifth SiC region) 26, a p++-type contact region 28, a first high concentration region of a p++-type (fourth SiC region) 30.

[0014]The SiC layer 10 includes a first surface and a second surface which faces the first surface. In FIG. 1, the first surface is a surface on an upper side of FIG. 1, and the second surface is a surface on a lower side of FIG. 1. Hereinafter, the first surface is referred to as a front surface, and the second surface is referred to as a rear surface.

[0015]The SiC layer 10 is, for example, a single crystal SiC (silicon carbide) of a 4H-SiC structure. A thickness of the SiC layer 10 is, for example, greater than or equal to 5 mm and smaller than or equal to 600 mm.

[0016]The n+-type cathode region 18 is provided on the second surface of the SiC layer 10. The cathode region 18 contains n-type impurity. The n-type impurity is, for example, nitride (N). Impurity concentration of the n-type impurity is, for example, higher than or equal to 1´1018 cm-3 and lower than or equal to 1´1020 cm-3.

[0017]The n--type drift region (first SiC region) 20 is provided on the cathode region 18. A part of the n--type drift region 20 is provided on an front surface of the element region. The drift region 20 contains n-type impurity. The n-type impurity is, for example, nitride (N). Impurity concentration of the n-type impurity is, for example, higher than or equal to 5´1014 cm-3 and lower than or equal to 1´1017 cm-3.

[0018]The p+-type edge region (second SiC region) 22 is provided such that at least a part thereof surrounds a region 40 (region surrounded by a dotted line of FIG. 2) in which the anode electrode 12 and the front surface of the SiC layer 10 come into contact with each other. The edge region 22 is provided between the drift region 20 and the front surface of the SiC layer 10. The edge region 22 is provided so as to surround the element region.

[0019]The edge region 22 contains p-type impurity. The p-type impurity is, for example, aluminum (Al). The impurity concentration of the p-type impurity is, for example, higher than or equal to 5´1017 cm-3 and lower than or equal to 5´1019 cm-3.

[0020]The first RESURF region of a p-type (third SiC region) 24 is provided so as to surround the edge region 22. The first RESURF region 24 is provided between the drift region 20 and the front surface of the SiC layer 10. The edge region 22 and the first RESURF region 24 come into contact with each other.

[0021]The first RESURF region 24 contains p-type impurity. The p-type impurity is, for example, aluminum (Al). Impurity concentration of the p-type impurity of the first RESURF region 24 is lower than impurity concentration of the p-type impurity of the edge region 22. Impurity concentration of the p-type impurity is, for example, higher than or equal to 5´1016 cm-3 and lower than or equal to 1´1018 cm-3.

[0022]The second RESURF region a p-type (fifth SiC region) 26 is provided so as to surround the first RESURF region 24. The second RESURF region 26 is provided between the drift region 20 and the front surface of the SiC layer 10. The first RESURF region 24 and the second RESURF region 26 come into contact with each other.

[0023]The second RESURF region 26 contains p-type impurity. The p-type impurity is, for example, aluminum (Al). Impurity concentration of the p-type impurity of the second RESURF region 26 is lower than impurity concentration of the p-type impurity of the first RESURF region 24. Impurity concentration of the p-type impurity is, for example, higher than or equal to 1´1016 cm-3 and lower than or equal to 1´1018 cm-3.

[0024]The p++-type contact region 28 is provided in the edge region 22. The p++-type contact region 28 is provided between the edge region 22 and the front surface of the SiC layer 10. The p++-type contact region 28 is provided so as to come into contact with the front surface of the SiC layer 10.

[0025]The p++-type contact region 28 contains p-type impurity. The p-type impurity is, for example, aluminum (Al). Impurity concentration of the p-type impurity of the p++-type contact region 28 is higher than impurity concentration of the p-type impurity of the edge region 22. Impurity concentration of the p-type impurity is, for example, higher than or equal to 1´1019 cm-3 and lower than or equal to 1´1021 cm-3.

[0026]The first high concentration region of p++-type (fourth SiC region) 30 is provided between the edge region 22 and the first RESURF region 24. The first high concentration region 30 is provided in a boundary portion between the edge region 22 and the first RESURF region 24. The first high concentration region 30 has a pattern of a ring shape which surrounds the edge region 22. The first high concentration region 30 comes into contact with the edge region 22 and the first RESURF region 24.

[0027]The first high concentration region 30 contains p-type impurity. The p-type impurity is, for example, aluminum (Al). Impurity concentration of the p-type impurity of the first high concentration region 30 is higher than impurity concentration of the p-type impurity of the edge region 22 and the first RESURF region 24.

[0028]A depth in which a front surface of the SiC layer 10 of the first high concentration region 30 is used as a reference is smaller than a depth in which a front surface of the SiC layer 10 of the edge region 22 and the first RESURF region 24 is used as a reference. A depth of the first high concentration region 30 is, for example, greater than or equal to 0.05 mm and smaller than or equal to 1.0 mm. Depths of the edge region 22 and the first RESURF region 24 are, for example, greater than or equal to 0.1 mm and smaller than or equal to 1.0 mm.

[0029]Impurity concentration of the SiC layer 10 can be measured by using a secondary ion mass spectrometry (SIMS) method. In addition, a relative level of the impurity concentration can also be determined from a level of a carrier concentration which is obtained by, for example, a scanning capacitance microscopy (SCM). In addition, a depth of an impurity region can be obtained by, for example, the SIMS. In addition, the depth of the impurity region can be obtained from, for example, a synthetic image of an SCM image and an atomic force microscopy (AFM) image.

[0030]The field oxide film 16 is provided on the front surface of the SiC layer 10. The field oxide film 16 is provided on the edge region 22, the first RESURF region 24, the second RESURF region 26, and the first high concentration region 30.

[0031]The field oxide film 16 includes an opening in the element region. The field oxide film 16 is, for example, a silicon oxide film. A thickness the field oxide film 16 is, for example, greater than or equal to 0.01 mm and smaller than or equal to 10 mm.

[0032]The anode electrode (first electrode) 12 comes into contact with the drift region 20, the edge region 22, and the contact region 28, in an opening of the field oxide film 16. Contact between the anode electrode 12 and the drift region 20 is Schottky contact. It is preferable that contact between the anode electrode 12 and the contact region 28 is Ohmic contact.

[0033]The anode electrode 12 is a metal. The anode electrode 12 is, for example, a laminated film of titanium (Ti) and aluminum (Al).

[0034]The cathode electrode 14 is provided so as to come into contact with the rear surface of the SiC layer 10. The cathode electrode 14 is provided so as to come into contact with the cathode region 18. It is preferable that contact between the cathode electrode 14 and the cathode region 18 is an Ohmic contact.

[0035]The cathode region 18 includes a metal. The cathode region 18 is configured by, for example, a laminated film of nickel silicide and a metal.

[0036]Next, actions and effects of the SBD 100 will be described.

[0037]In the vertical SBD, when a reverse bias is applied, if avalanche breakdown occurs in an end portion of the element region by an electric field which is concentrated in the end portion of the element region, element breakdown easily occurs and avalanche resistance decreases. In order to reduce concentration of the electric field in the end portion of the element region, for example, a p-type RESURF region is provided in the termination region in the periphery of the element region. Since the p-type RESURF region is depleted, strength of the electric field strength which is applied to the end portion of the element region is reduced, avalanche breakdown hardly occur in the end portion of the element region, and avalanche resistance of the SBD increases.

[0038]However, by providing the p-type RESURF region, a p-type region in the termination region becomes, for example, a multistage structure of the p+-type edge region and the p-type RESURF region. Then, an electric field is concentrated in a place in which impurity concentration of p-type impurity changes, and thereby electric field strength increases. Hence, avalanche breakdown occurs in the place, and there is possibility that sufficient avalanche resistance is not obtained.

[0039]If the multistage structure of the concentration of the p-type region is formed by ion injection by which the amount of dose is changed and annealing, impurity concentration of the p-type impurity is rapidly changed particularly in SiC. The reason is that impurity diffusion in SiC is much slower than that in, for example, silicon (Si). If aluminum (Al) is used as p-type impurity, impurity concentration of the p-type impurity is rapidly changed in particular, because a diffusion coefficient in the SiC is extremely small.

[0040]If the impurity concentration is rapidly changed, electric field strength increases. In order to more increase the avalanche resistance of the SBD, it is preferable that the electric field strength is reduced in a place in which impurity concentration of the p-type impurity is changed.

[0041]In the SBD 100 according to the present embodiment, the first high concentration region 30 with higher impurity concentration of p-type impurity than those in the edge region 22 and the first RESURF region 24 is provided in a boundary portion between the edge region 22 in which impurity concentration of p-type impurity is changed, and the first RESURF region 24.

[0042]By providing the first high concentration region 30, when a reverse bias is applied to the SBD 100, a leakage current flows between the edge region 22 and the first RESURF region 24. The electric field strength of the boundary portion between the edge region 22 and the first RESURF region 24 is reduced by a voltage drop due to the leakage current. Hence, avalanche breakdown hardly occurs in the boundary portion between the edge region 22 and the first RESURF region 24. Thus, the avalanche resistance of the SBD 100 increases. The leakage is caused by impurity concentration of the high p-type impurity of the first high concentration region 30, and crystal defect which is generated when the first high concentration region 30 is formed.

[0043]It is preferable that a depth of the SiC layer 10 of the first high concentration region 30 is smaller than depths of the edge region 22 and the first RESURF region 24. If the depth of the first high concentration region 30 is deep, there is possibility that the first high concentration region 30 comes into contact with the drift region 20, and a leakage current at the time of reverse bias of the SBD 100 increases.

[0044]In addition, it is preferable that impurity concentration of the p-type impurity of the first high concentration region 30 is higher than impurity concentration of the p-type impurity of the edge region 22 by one digit or more, from a viewpoint in which electric field strength of the boundary portion between the edge region 22 and the first RESURF region 24 is reduced. In addition, it is preferable that impurity concentration of the p-type impurity of the first high concentration region 30 is higher than or equal to 1´1020 cm-3.

[0045]As such, according to the SBD 100 according to the present embodiment, the electric field strength in the termination region is reduced, and thereby an increase of the avalanche resistance is realized.

Second Embodiment

[0046]A semiconductor device according to the present embodiment is different from the semiconductor device according to the first embodiment in that the first high concentration region of a p++-type (fourth SiC region) 30 also serves as a p++-type contact region. Hereinafter, a part of description of contents that overlap the first embodiment will be omitted.

[0047]FIG. 3 is a schematic sectional view of a semiconductor device according to the present embodiment. The semiconductor device according to the present embodiment is an SBD 200.

[0048]In the SBD 200, the anode electrode 12 comes into contact with the first high concentration region of a p++-type (fourth SiC region) 30. The first high concentration region 30 also serves as a contact region for reducing a contact resistance of the anode electrode 12.

[0049]According to the SBD 200 according to the present embodiment, electric field strength in the termination region is reduced and an increase of avalanche resistance is realized by the same actions as in the first embodiment.

Third Embodiment

[0050]A semiconductor device according to the present embodiment is different from the semiconductor device according to the first embodiment in that the depth in which the first surface of the fourth SiC region is used as a reference is greater than or equal to the depth in which the first surface of the second SiC region and the third SiC region is used as a reference. Hereinafter, a part of description of contents that overlap the first embodiment will be omitted.

[0051]FIG. 4 is a schematic sectional view of a semiconductor device according to the present embodiment. The semiconductor device according to the present embodiment is an SBD 300.

[0052]In the SBD 300, the depth in which the front surface of the SiC layer 10 of the first high concentration region 30 is used as a reference is equal to, or greater than the depth in which the front surface of the SiC layer 10 of the edge region 22 and the first RESURF region 24 is used as a reference.

[0053]According to the SBD 300 according to the present embodiment, electric field strength in the termination region is reduced and an increase of avalanche resistance is realized by the same actions as in the first embodiment.

Fourth Embodiment

[0054]A semiconductor device according to the present embodiment is different from the semiconductor device according to the first embodiment in that a second high concentration region is provided between the third SiC region and the fifth SiC region. Hereinafter, a part of description of contents that overlap the first embodiment will be omitted.

[0055]FIG. 5 is a schematic sectional view of a semiconductor device according to the present embodiment. The semiconductor device according to the present embodiment is an SBD 400.

[0056]The SBD 400 includes a second high concentration region of a p+-type 32. The second high concentration region of a p+-type 32 is provided between the first RESURF region 24 and the second RESURF region 26. The second high concentration region 32 is provided in a boundary portion between the first RESURF region 24 and the second RESURF region 26. The second high concentration region 32 has a ring pattern which surrounds the first RESURF region 24.

[0057]The second high concentration region 32 contains p-type impurity. The p-type impurity is, for example, aluminum (Al). Impurity concentration of the p-type impurity of the second high concentration region 32 is higher than impurity concentration of the p-type impurity of the first RESURF region 24 and the second RESURF region 26.

[0058]A depth in which a front surface of the SiC layer 10 of the second high concentration region 32 is used as a reference is smaller than the depth in which the front surface of the SiC layer 10 of the first RESURF region 24 and the second RESURF region 26 is used as a reference. The depth of the second high concentration region 32 is, for example, greater than or equal to 0.05 mm and smaller than or equal to 1.0 mm. The depths of the first RESURF region 24 and the second RESURF region 26 are, for example, greater than or equal to 0.1 mm and smaller than or equal to 1.0 mm.

[0059]Electric field strength of the boundary portion between the first RESURF region 24 and the second RESURF region 26 is reduced by providing the second high concentration region 32. Hence, avalanche breakdown in the boundary portion between the first RESURF region 24 and the second RESURF region 26 hardly occurs. Thus, avalanche resistance of the SBD 400 increases.

[0060]According to the SBD 400 according to the present embodiment, electric field strength in the termination region is reduced and an increase of avalanche resistance is realized by the same actions as in the first embodiment.

Fifth Embodiment

[0061]A semiconductor device according to the present embodiment is different from the semiconductor device according to the first embodiment in that a shape of the first surface of the fourth SiC region is not a ring shape and an island shape. Hereinafter, a part of description of contents that overlap the first embodiment will be omitted.

[0062]FIG. 6 is a schematic sectional view of a semiconductor device according to the present embodiment. FIG. 6 illustrates a pattern of impurity region on the semiconductor device. The semiconductor device according to the present embodiment is an SBD 500.

[0063]As illustrated in FIG. 6, in the SBD 500, the first high concentration region 30 has a pattern of an island shape which is provided between the edge region 22 and the first RESURF region 24, on the front surface of the SiC layer 10.

[0064]According to the SBD 500 according to the present embodiment, electric field strength in the termination region is reduced and an increase of avalanche resistance is realized by the same actions as in the first embodiment.

Sixth Embodiment

[0065]A semiconductor device according to the present embodiment is different from the semiconductor device according to the first embodiment in that the semiconductor device according to the present embodiment is a PIN diode which includes a p-type anode region between the first surface of the SiC layer and the first SiC region. Hereinafter, a part of description of contents that overlap the first embodiment will be omitted.

[0066]FIG. 7 is a schematic sectional view of a semiconductor device according to the present embodiment. The semiconductor device according to the present embodiment is a PIN diode 600.

[0067]The PIN diode 600 includes a p+-type anode region 34. The anode electrode 12 is electrically coupled to the anode region 34. The p+-type anode region 34 comes into contact with the edge region 22.

[0068]The p+-type anode region 34 contains p-type impurity. The p-type impurity is, for example, aluminum (Al). Impurity concentration of the p-type impurity is, for example, higher than or equal to 1´1018 cm-3 and lower than or equal to 1´1019 cm-3.

[0069]The p++-type contact region 28 is provided between the anode electrode 12 and the anode region 34. The anode electrode 12 comes into contact with the p++-type contact region 28.

[0070]A structure of the termination region is the same as in the first embodiment.

[0071]According to the PIN diode 600 according to the present embodiment, electric field strength in the termination region is reduced and an increase of avalanche resistance is realized by the same actions as in the first embodiment.

Seventh Embodiment

[0072]A semiconductor device according to the present embodiment is different from the semiconductor device according to the first embodiment in that the semiconductor device according to the present embodiment is a MOSFET. Hereinafter, a part of description of contents that overlap the first embodiment will be omitted.

[0073]FIG. 8 is a schematic sectional view of a semiconductor device according to the present embodiment. The semiconductor device according to the present embodiment is a metal oxide semiconductor field effect transistor (MOSFET) 700.

[0074]In the MOSFET 700, an element region includes a p-type body region 42 which is provided on a front surface of the SiC layer 10, an n+-type source region 44, a gate insulating film 46, a gate electrode 48, an interlayer film 50, an n+-type drain region 19, a source electrode (first electrode) 13, a drain electrode (second electrode) 15.

[0075]The source electrode (first electrode) 13 is electrically coupled to the body region 42, the source region 44. The source electrode (first electrode) 13 comes into contact with 44. The gate electrode 48 and the source electrode 13 are insulated with each other by the interlayer film 50.

[0076]A structure of the termination region is the same as in the first embodiment.

[0077]According to the MOSFET 700 according to the present embodiment, electric field strength in the termination region is reduced and an increase of avalanche resistance is realized by the same actions as in the first embodiment.

Eighth Embodiment

[0078]A semiconductor device according to the present embodiment includes a SiC layer which includes a first surface and a second surface; a first electrode which comes into contact with the first surface; a first SiC region of a first conductive type which is provided in the SiC layer; a second SiC region of the second conductive type which is provided in the SiC layer such that at least a part of the second SiC region surrounds a region which comes into contact with the first electrode and the first surface, and is provided between the first SiC region and the first surface; a third SiC region of a second conductive type which is provided in the SiC layer so as to surround the second SiC region, is provided between the first SiC region and the first surface, and contains lower impurity concentration of the second conductive type than that of the second SiC region; and a fourth SiC region which is provided in the SiC layer between the second SiC region and the third Sic region, and has higher crystal defect density than those of the second SiC region and the third Sic region. A semiconductor device according to the present embodiment is different from the semiconductor device according to the first embodiment in that the fourth SiC region is a region with high crystal defect density. Hereinafter, a part of description of contents that overlap the first embodiment will be omitted.

[0079]FIG. 9 is a schematic sectional view of a semiconductor device according to the present embodiment. The semiconductor device according to the present embodiment is an SBD 800.

[0080]The SBD 800 includes an element region and a termination region which surrounds the element region. The element region functions as a region through which a current mainly flows at the time of a forward bias of the SBD 800. The termination region has a termination structure in which strength of an electric field that is applied to an end portion of the element region is reduced at the time of a reverse bias of the SBD 800, and an element breakdown voltage of the SBD 800 increases.

[0081]The SBD 800 includes the SiC layer 10, the anode electrode 12, the cathode electrode 14, and a field oxide film 16. An n+-type cathode region 18, an n--type drift region (first SiC region) 20, a p+- edge region (second SiC region) 22, a first RESURF region of a p-type (third SiC region) 24, a second RESURF region of a p—type (fifth SiC region) 26, a p++-type contact region 28, a high defect density region (fourth SiC region) 60 are provided in the SiC layer 10.

[0082]The SiC layer 10 includes a first surface and a second surface which faces the first surface. In FIG. 9, the first surface is a surface on an upper side of FIG. 1, and the second surface is a surface on a lower side of FIG. 1. Hereinafter, the first surface is referred to as a front surface, and the second surface is referred to as a rear surface.

[0083]The high defect density region (fourth SiC region) 60 is provided between the edge region 22 and the first RESURF region 24. The high defect density region 60 is provided in a boundary portion between the edge region 22 and the first RESURF region 24. The high defect density region 60 has, for example, a ring pattern which surrounds the edge region 22.

[0084]The high defect density region 60 has higher crystal defect density than those of the edge region 22 and the first RESURF region 24. The high defect density region 60 is formed by ion injection of, for example, argon (Ar). The high defect density region 60 includes, for example, argon (Ar).

[0085]A depth in which a front surface of the SiC layer 10 of the high defect density region 60 is used as a reference is smaller than the depth in which a front surface of the SiC layer 10 of the edge region 22 and the first RESURF region 24 is used as a reference. A depth of the high defect density region 60 is, for example, greater than or equal to 0.05 mm and smaller than or equal to 1.0 mm. Depths of the edge region 22 and the first RESURF region 24 are, for example, greater than or equal to 0.1 mm and smaller than or equal to 1.0 mm.

[0086]Crystal defect density of the high defect density region 60 and crystal defect density of the edge region 22 and the first RESURF region 24 can be compared to each other by, for example, a transmission electron microscope (TEM). Whether or not the high defect density region 60 contains argon (Ar) can be determined by, for example, a SIMS.

[0087]By providing the high defect density region 60, when a reverse bias is applied to the SBD 800, a leakage current due to crystal defect flows between the edge region 22 and the first RESURF region 24. The electric field strength of the boundary portion between the edge region 22 and the first RESURF region 24 is reduced by a voltage drop due to the leakage current. Hence, avalanche breakdown hardly occurs in the boundary portion between the edge region 22 and the first RESURF region 24. Thus, breakdown voltage of the SBD 800 increases.

[0088]It is preferable that the depth of the SiC layer 10 of the high defect density region 60 is smaller than the depths of the edge region 22 and the first RESURF region 24. If the depth of the high defect density region 60 is deep, the high defect density region 60 comes into contact with the drift region 20, and there is possibility that the leakage current at the time of a reverse bias of the SBD 800 increases.

[0089]As such, according to the SBD 800 according to the present embodiment, electric field strength in the termination region is reduced and thereby an increase of avalanche resistance is realized.

[0090]In the first to eighth embodiments, a case in which 4H-SiC is used as a crystal structure of SiC is described as an example, but exemplary embodiments can also be applied to a device which uses SiC with other crystal structures such as, 6H-SiC or 3C-SiC

[0091]In addition, in the embodiments, an example in which a SBD, a PIN diode, and a MOSFET are mainly used is described, but exemplary embodiments can also be applied to other devices such as, a metal insulator semiconductor field effect transistor (MISFET) or an insulated gate bipolar transistor (IGBT), as long as the device includes a termination region in the periphery of an element region.

[0092]In addition, in the embodiments, a case in which the first conductive type is an n-type and the second conductive type is a p-type is described, but the first conductive type may be a p-type and the second conductive type may be an n-type.

[0093]While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the novel embodiments described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the inventions.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a SiC layer which includes a first surface and a second surface;

a first electrode which comes into contact with the first surface;

a first SiC region of a first conductive type which is provided in the SiC layer;

a second SiC region of the second conductive type which is provided in the SiC layer such that at least a part of the second SiC region surrounds a region which comes into contact with the first electrode and the first surface, and is provided between the first SiC region and the first surface;

a third SiC region of a second conductive type which is provided in the SiC layer so as to surround the second SiC region, is provided between the first SiC region and the first surface, and contains lower impurity concentration of the second conductive type than that of the second SiC region; and

a fourth SiC region of the second conductive type which is provided in the SiC layer between the second SiC region and the third Sic region, and contains higher impurity concentration of the second conductive type than that of the second SiC region.

2. The device according to Claim 1, further comprising:

a second electrode which is provided in the second surface.

3. The device according to Claim 1 or 2, wherein the first electrode is electrically coupled to the second Sic region.

4. The device according to any one of Claims 1 to 3, wherein the fourth Sic region surrounds the second SiC region.

5. The device according to any one of Claims 1 to 4, wherein a depth in which the first surface of the fourth SiC region is used as a reference is smaller than a depth in which the first surface of the second SiC region and the third SiC region is used as a reference.

6. The device according to any one of Claims 1 to 5, wherein the second SiC region comes into contact with the third SiC region.

7. The device according to any one of Claims 1 to 6, further comprising:

a fifth SiC region which is provided in the SiC layer so as to surround the third SiC region, is provided between the first SiC region and the first surface, and contains lower impurity concentration of the second conductive type than that of the third SiC region.

8. The device according to any one of Claims 1 to 7, wherein the second SiC region, the third SiC region, and the fourth SiC region contain aluminum (Al).

9. A semiconductor device comprising:

a SiC layer which includes a first surface and a second surface;

a first electrode which comes into contact with the first surface;

a first SiC region of a first conductive type which is provided in the SiC layer;

a second SiC region of the second conductive type which is provided in the SiC layer such that at least a part of the second SiC region surrounds a region which comes into contact with the first electrode and the first surface, and is provided between the first SiC region and the first surface;

a third SiC region of a second conductive type which is provided in the SiC layer so as to surround the second SiC region, is provided between the first SiC region and the first surface, and contains lower impurity concentration of the second conductive type than that of the second SiC region; and

a fourth SiC region of the second conductive type which is provided in the SiC layer between the second SiC region and the third Sic region, and has higher crystal defect density than those of the second SiC region and the third Sic region.

10. The device according to Claim 9, further comprising:

a second electrode which is provided in the second surface.

11. The device according to Claim 9 or 10, wherein the first electrode is electrically coupled to the second Sic region.

12. The device according to any one of Claims 9 to 11, wherein the fourth Sic region surrounds the second SiC region.

13. The device according to any one of Claims 9 to 12, wherein the fourth Sic region contains argon (Ar).

ABSTRACT

According to one embodiment, a semiconductor device includes a SiC layer which includes a first surface and a second surface; a first electrode which comes into contact with the first surface; a first SiC region of a first conductive type which is provided in the SiC layer; a second SiC region of the second conductive type which is provided in the SiC layer such that at leasta part of the second SiC region surrounds a region which comes into contact with the first electrode and the first surface, and is provided between the first SiC region and the first surface; a third SiC region of a second conductive type which is provided in the SiC layer so as to surround the second SiC region, is provided between the first SiC region and the first surface, and contains lower impurity concentration of the second conductive type than that of the second SiC region; and a fourth SiC region of the second conductive type which is provided in the SiC layer between the second SiC region and the third Sic region, and contains higher impurity concentration of the second conductive type than that of the second SiC region.

DRAWINGS

FIG. 1

TERMINATION REGION

ELEMENT REGION

TERMINATION REGION

FIRST SURFACE

SECOND SURFACE

FIG. 3

TERMINATION REGION

ELEMENT REGION

TERMINATION REGION

FIRST SURFACE

SECOND SURFACE

FIG. 4

TERMINATION REGION

ELEMENT REGION

TERMINATION REGION

FIRST SURFACE

SECOND SURFACE

FIG. 5

TERMINATION REGION

ELEMENT REGION

TERMINATION REGION

FIRST SURFACE

SECOND SURFACE

FIG. 7

TERMINATION REGION

ELEMENT REGION

TERMINATION REGION

FIRST SURFACE

SECOND SURFACE

FIG. 8

TERMINATION REGION

ELEMENT REGION

TERMINATION REGION

FIRST SURFACE

SECOND SURFACE

FIG. 9

TERMINATION REGION

ELEMENT REGION

TERMINATION REGION

FIRST SURFACE

SECOND SURFACE